UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/937,194	09/21/2001	Seiji Ohno	NSG-201US	6387

23122 7590 11/14/2002

RATNERPRESTIA
P O BOX 980
VALLEY FORGE, PA 19482-0980

EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/937,194	OHNO ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on th cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-7 and 9-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-7 and 9-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The corrected or substitute drawing of Figure 1 was received on 08/27/2002. This drawing is accepted.

Specification

Although it is clear from the Declaration that the application is a national stage of a PCT application, this should be pointed out in the first page of the specification as well.

Response to Amendment

Amendment A filed 08/27/2002 and entered as Paper No. 7 forms the basis of the present Office Action. In Amendment A Applicant canceled claims 2, 3 and 8 and substantially amended all remaining claims through a substantial amendment of the independent claims 1 and 7, and in addition through substantial amendment of dependent claims 4-6 and 9-12. Comments on Remarks by Applicant as found below in "Response to Arguments" are therefore restricted to those aspects that still are pertinent to the present claim set.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant (henceforth called "APA") in view of Kamei (JP359117280A) and Sonobe et al (US 2002/0153532 A1).

With regard to claim 1: As shown in the disclosure on pages 2 and 3, and as illustrated in Figure 1, APA teaches a light-emitting thyristor matrix array formed on a chip (page 2, lines 7-8 and page 3, line 9) comprising: N (N being an integer > 1) three-terminal (anode, cathode, gate) light-emitting thyristors (page 2, lines 9, 12, 14, and 16) in one line (page 2, line 10) in parallel with the long side of the chip (all thyristors are positioned on said chip while they are aligned with (along) the long side of the chip); and a plurality of bonding pads also formed on the chip (cf. page 3, line 8-10). The light-emitting thyristor taught by APA further comprises: a common terminal to which cathodes are of the N light-emitting thyristors are connected (indicated "K" on Figure 1 and page 2, lines 15-16); and M (M=4>1) gate-selecting lines (cf. Figure 1 and page 2, lines 17-20); wherein the gate of the k-th light-emitting thyristor is connected the i-th (modulus M=4) gate-selecting line G_i, the anode being connected to the j-th anode terminal A_j, where j= (k-i)/M +1.

APA does not necessarily teach the plurality of bonding pads to be arrayed in one line in parallel with the long side of the chip. However, Kamei teaches a plurality of bonding pads arrayed in one line in parallel with the long side of the chip, namely bonding pads 9a (Figures 1 and 2). The purpose of Kamei, namely to facilitate adjusting the trimming (adjusting the light amount) through a separate bonding pad 9a for each light-emitting element 5, enabling the option of separate re-connecting of any light-

emitting element to an alternative bonding pad (bonding pads 9b, 9c, etc..), is a valid *motivation* also for the invention disclosed as Prior Art admitted by Applicant because the intensities of different printing lines should ideally be the same. Furthermore, the distance between each light-element 5 and its bonding pad 9a, casu quo alternative bonding pads 9b, 9c,.., is kept minimal by means of the alignment of bonding pads 9a in parallel with the light-element array. Although Kamei does not necessarily teach the plurality of bonding pads to be a plurality of {M/N+M} bonding pads. However, APA teaches {N/M + M} control terminals (namely M control terminals for the M gate selecting lines and one control terminal for each of the N/M sub-groups of thyristors) in the conventional art as disclosed on page 2 of the disclosure (lines 25-30), while Sonobe et al teach that, for decreasing the area of the control circuit substrate (cf. section [0020]), each control terminal 3c is folded in an L-shape to correspond or form a bonding pad 4c (cf. section [0076]). Sonobe et al thereby make it obvious that the number of bonding pads should equal the number of control terminals in the invention of Kamei in order to improve the capitalization of surface area while preserving the integrity of the connections.

Finally, the light-emitting thyristor essentially taught by APA in view of Kamei satisfies the further limitation of the final four lines of claim 1 as Kamei shows that there is ample room for (at least) one more bond pad to be placed on the chip, and thus the length L exceeds the product of the number of bond pads and the pitch of the bond pad array by more than one bond array pitch. It is understood in the art that to place the

absolute maximum number of elements in an array as allowed by the length of the chip would place the outer elements arbitrarily close to outside influence.

The inventions can be straightforwardly *combined* in as far as the relevant aspects of the teachings by Kamei and Sonobe et al are concerned, because the linear array of light-emitting elements as taught by the APA is simply the first step in the manufacturing process for the end product. Reasonable expectation of success is ensured by the absence of any unknown elements in the manufacturing process and in the independence of the fabrication of the array of light-emitting elements and the array of bonding pads.

With regard to claim 4: An optimum or range as expressed in this claim by the phrase "about 75 μm" is not necessarily taught by APA, nor by Kamei, nor by Sonobe et al. However, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

With regard to claims 5 and 6: the number M of gate-selecting lines as taught by APA (Figure 1 of disclosure) is 4, which is the third integer starting from the smallest possible choice of 2.

With regard to claim 12: Any of the claims 2-6 are unpatentable over APA in view of Kamei and Sonobe et al, as explained above. Although a driver circuit has not necessarily been disclosed as APA nor by Kamei nor by Sonobe et al, a driver circuit for the aforementioned gate-selecting lines as well as a driver circuit for driving the aforementioned anode terminals are necessary for these gate-selecting lines and anode

terminals to function. It is equally obvious that the very process of selecting a gate to receive a signal implies for the relevant circuit to output a "selecting" signal to one of the gate-selecting signal output terminals and a "no-selecting" signal to the other gate-selecting signal output terminals, with the terminal to which the "selecting" signal is supplied being switched in turn. The very meaning of the word "selecting" suffices here.

2. ***Claims 7-11*** are rejected under 35 U.S.C. 103(a) as being unpatentable over APA, Kamei, Sonobe et al, and Breeze (4,394,653).

With regard to claim 7: On those features that are common between claims 1 and 7 please be referred to the reasons for rejection of claim 1 as amply expanded above. Neither APA nor Kamei necessarily teach the specific limitation of claim 7 not included in claim 1. However, in the art of light-emitting element arrays for image display systems (cf. title and abstract), hence closely related to the art of the invention, Breeze teaches (cf. Fig. 3) LED arrays in which a there is a spatial period characterized by a fixed number of adjacent LEDs, each member of said fixed number of LEDs corresponding to a different image (cf. column 2, line 38 – column 3, line 6); the total image is then a superposition of images produced by the members of said fixed number of LEDs, while image selection is carried out through the anode voltage selection (cf. Fig. 3; cf. column 4, line 66 – column 5, line 63). The anode connection is different for every different member of said fixed number of LEDs, i.e., within the spatial period, while the gates within the period are interconnected ohmically. For the usefulness of the invention as taught by APA in view of Kamei as defined in claim 1 for the purpose of image display it

therefore would be obviously advantageous to have separate anodes but a common gate within the LED periodic unit responsible for the display of one character. Therefore, there is ample *motivation* to combine the inventions. Identically the same advantageous spatial arrangement of electrical connections with the aim of reducing connection requirements on spatial resources would be achieved when the commonality of the anode would be replaced by the commonality of the gate. The inventions can be *combined*: all that needs to be done is to *interchange* anode and gate connections without loss of said spatial resources. *Reasonable expectation of success is ensured* keeping in mind the relative simplicity involved in the interchange.

In conclusion, it would have been obvious to one of ordinary skills in the art to modify the invention of claim 1 (as essentially taught by APA and Kamei) so as to include the further limitation as defined by claim 7.

With regard to claim 8: the light-emitting thyristor essentially taught by APA in view of Kamei and Sonobe et al satisfies claim 8 as Figures 1 and 3 in Kamei show that there is ample room for (at least) one more bond pad to be placed on the chip, and thus the length L exceeds the product of the number of bond pads and the pitch of the bond pad array by more than one bond array pitch. It is understood in the art that to place the absolute maximum number of elements in an array as allowed by the length of the chip would place the outer elements arbitrarily close to outside influence.

With regard to claim 9: An optimum or range as expressed in this claim by the phrase "about 75 μm" is not necessarily taught by APA nor by Kamei. However, it has been held that where the general conditions of a claim are disclosed in the prior art,

discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

With regard to claims 10 and 11: the number M of gate-selecting lines as taught by APA (Figure 1 of disclosure) is 4, which is the third integer starting from the smallest possible choice of 2.

3. ***Claims 13-14*** are rejected under 35 U.S.C. 103(a) as being unpatentable over APA, Kamei and Sonobe et al as applied to claim 12 above, and further in view of Mead et al (5,763,909). Although neither APA nor Kamei nor Sonobe disclose the further limitation as defined in claim 13 it is understood that the selection of parallel or serial input / output registers is a matter of design choice, as discussed by Mead et al in connection with a phototransistor imaging system, hence in the field of the invention (cf. title, abstract and column 10, lines 1-14) while, in connection with claim 14 the number of the gate-selecting signal output signal terminals in APA must be four since there are four gate-selecting lines.

Response to Arguments

4. Applicant's arguments filed 08/27/2002 have been fully considered but they are not persuasive. In particular, what Applicant calls the "Decreased Chip Area Feature" actually is nothing but the inequality involving "p" included in the claim language, which says nothing else but this" that the length available for the bonding pads on the chip should be exceeded by the chip length. This is truly a trivial relation, considering that the bonding pads have to fit, as explained in the previous office action, whether one places

said bonding pads on the chip or on a line parallel to the chip, as formulated in the actual claim language, in the latter case minimizing connection length; however, also keep in mind that the bonding pads in Kamei are formed on the resistor body which in turn is formed on the chip, and so the bonding pads are formed on the chip, counter to the allegation of Applicant in Remarks.

Furthermore, the newly introduced limitation that the plurality of bonding pads actually should number N/M+M is the mere statement that the number of bonding pads should be equal to the number of control terminals as disclosed by the prior art as admitted by Applicant (APA); see page 2 of the disclosure, lines 25-30. In fact, Sonobe et al disclose in a patent application on power semiconductor modules aiming to reduce the area of the control terminal substrate each control terminal should be folded into an L-shape to correspond with a bonding pad. This is exactly what Figure 11 of Applicant shows (Applicant's most clarifying figure), while it fulfills the requirement of the further limitation in claim 7. Motivation to include the teaching by Sonobe et al in this regard stems from the saving in space it would entail, in keeping with the objective of increasing chip area utilization in the prior art as admitted by Applicant (cf. pages 1-2 of the disclosure). In view of this circumstance, the "Bonding Pad Feature" of Applicant also should be considered unpatentable.

Parenthetically, it is noted that Patent "JP2807910", probably JP09-2807910, is still unavailable to the examiner.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
November 12, 2002

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800